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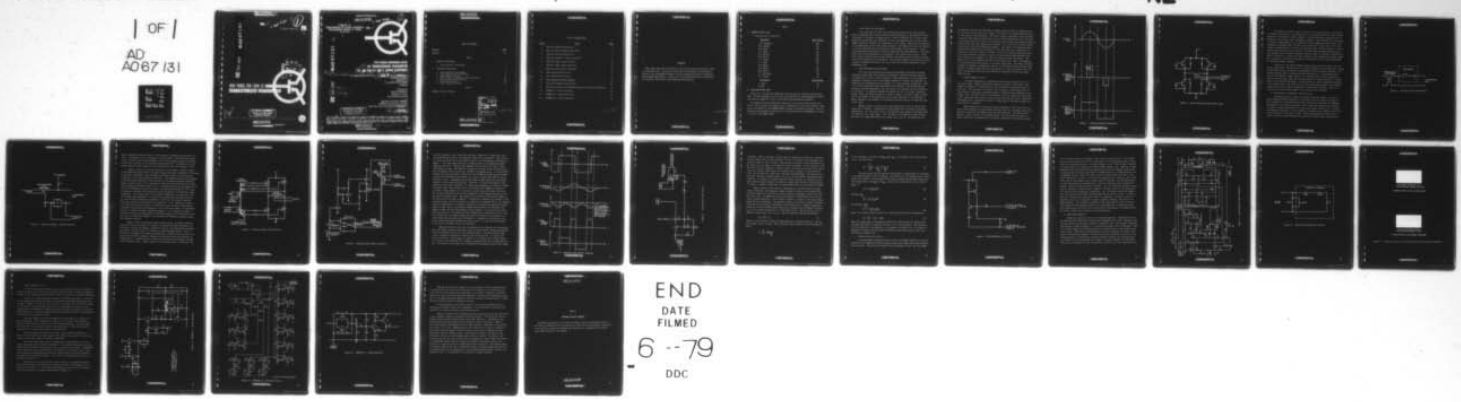

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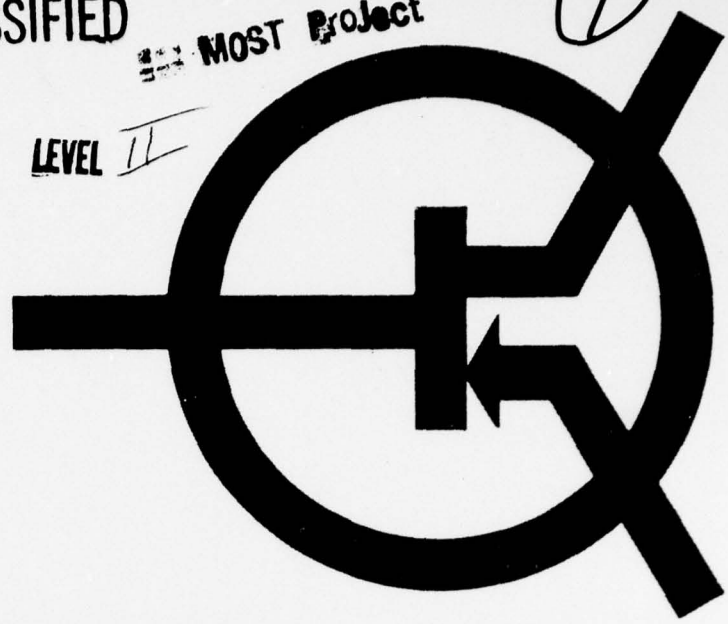

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FIFTH INTERIM ENGINEERING REPORT FOR TRANSISTORIZED TRANSMITTER FOR AN/SQS-26 (XN-2) SONAR EQUIPMENT

(6)

(9) Interim engineering rept. no 5,

This Report Covers the Period 1 JUL~~Y~~ ~~TO~~ 30 DECE~~MBER~~ 1961

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Prepared For
NAVY DEPARTMENT
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by
GENERAL ELECTRIC CO~~MPANY~~
DEFENSE ELECTRONICS DIVISION
HEAVY MILITARY ELECTRONICS ~~DEPARTMENT~~ Systems

(11) JAN~~UARY~~ 1962

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LIST OF ILLUSTRATIONS

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ABSTRACT

This report describes the progress on the contract during the period 1 July to 30 December 1961. During this period work was performed on the system described in the Recommendation Report that was submitted as part of the Fourth Interim Engineering Report. Authority to proceed with Phase III of the project was received. New circuits were developed and evaluated.

620421-0365

PART I

A. GENERAL FACTUAL DATA

1. Identification of Personnel

Engineers	Hours Worked
J.R. Greenbaum	840
A.M. Cashman	138
R.H. Riggs	337
A.L. Burns	112
D.A. Paynter	770
B.H. Rutter	328
J.V. O'Hern	832
F. King	229
V.P. Mathis	72
H.W. Abbott	104
R.W. French	282
A.V. Korolenko	28
H.J. Tucker	86

Lab Asst's	Hours Worked
I. Iback	68
H. Vail	64

B. DETAILED FACTUAL DATA

Authority to proceed with Phase III of the project was received during October 1962. The new equipment was to have the form described in the Recommendation Report that had been submitted as part of the Fourth Interim Engineering Report.

Two hundred and fifty modularized amplifiers and the associated circuitry required to drive twenty four staves are to be delivered in lieu of the complete transmitter replacement for the AN/SQS-26(XN-2) system as originally specified. The new transistorized transmitter modules are to be compatible with the AN/SQS-26( ) system to be built under NObsr-87002.

1. Output Amplifier Development

The output amplifier work during this reporting period has been concerned with the implementation of pulse width switching techniques in the amplifier for the development of 750 watts of signal power in a sonar transducer load. Various input signal driving methods were considered for use in the amplifier and the most advantageous method was selected for incorporation in the system. Effort was concentrated in the development of the output stage circuitry of the amplifier and in the selection of suitable semiconductors to perform the output stage circuit functions. A load coupling method was developed to suitably couple the switching amplifier to the transducer load, and TR switching was incorporated in the output load circuitry. Power level control circuitry and an output amplifier overload protection circuit was developed and incorporated in the amplifier. An extensive program of laboratory and field testing of breadboard versions of the new circuit was initiated during the circuit development work.

2. Pulse Width Switching Technique

Past work has shown that many desirable advantages result when switching techniques rather than linear methods are employed to develop substantial amounts of signal power to drive a sonar transducer. Chief among these is the reduced heat dissipation incurred in the active elements employed in a switch type amplifier as compared with corresponding active elements in a linear dissipation amplifier. This is of critical importance when semiconductors are employed. The reduced heating decreases internal temperatures, and this results in increased life and reliability of the device. A switching technique was adopted for use in the output amplifier design. Since the output voltage of a switch is equal to the switch supply voltage and is not related to the switch input drive signal amplitude, it is necessary to employ conduction time methods for controlling the switch output and hence the amplifier output.

Several methods of power control employing variable duty time switch techniques were considered. The method which was adopted had to satisfy the following requirements. (a) the output level of the amplifier must change in accordance with the amplitude of an input signal, (b) the phase of the amplifier output voltage wave must not change when power level changes occur, and (c) the method must be

economically feasible and preferably not employ auxiliary power switching devices for the power control functions. Figure 1 illustrates the voltage waveform present in the selected switching method. The switch timing is arranged so that the switch conduction time during any given half cycle is located symetrically about the peak of the input signal half cycle or stated another way has equal non-conduction periods centered about the input signal zero crossings. It is seen that the three requirements are met with this switching arrangement. The output of the amplifier may be varied from a maximum when W is equal to a full half cycle and a square wave is generated, down to zero when W is reduced to zero and no switch conduction occurs. It is only necessary to provide a circuit to convert input signal amplitude into pulse durations as in Figure 1 in order to satisfy the first requirement. The phase is seen to be preserved for all levels of power output due to the symmetry of conduction periods with respect to the input signal wave. The method satisfies economy of components considerations when it is considered that the switches which develop the output signal power are also employed to control the power level, and hence, no additional power switching devices are required to perform the power level function.

3. Output Stage Circuitry

A bridge configuration of switching transistors was selected for use in the output stage. Figure 2 illustrates the basic circuitry of the stage. The bridge is composed of 4 switching units each of which has a transistor and a bypass diode. The switches act in pairs so as to produce a bidirectional flow of load current in the output transformer primary, connected at the midpoints of the bridge. Thus, switches 1 and 4 are energized as a pair to produce one half cycle of the output wave, and switches 2 and 3 produce the other half cycle. Additional transistors may be connected in parallel to those shown if additional bridge current capacity is required.

Bridge operation of the output stage is desirable in that the circuit exhibits fewer transient voltage problems and allows the use of a higher supply voltage than is possible with conventional push-pull amplifiers. The output transformer is better utilized in the bridge circuit, and this permits the use of a smaller sized unit as compared with a push-pull transformer of equivalent rating.

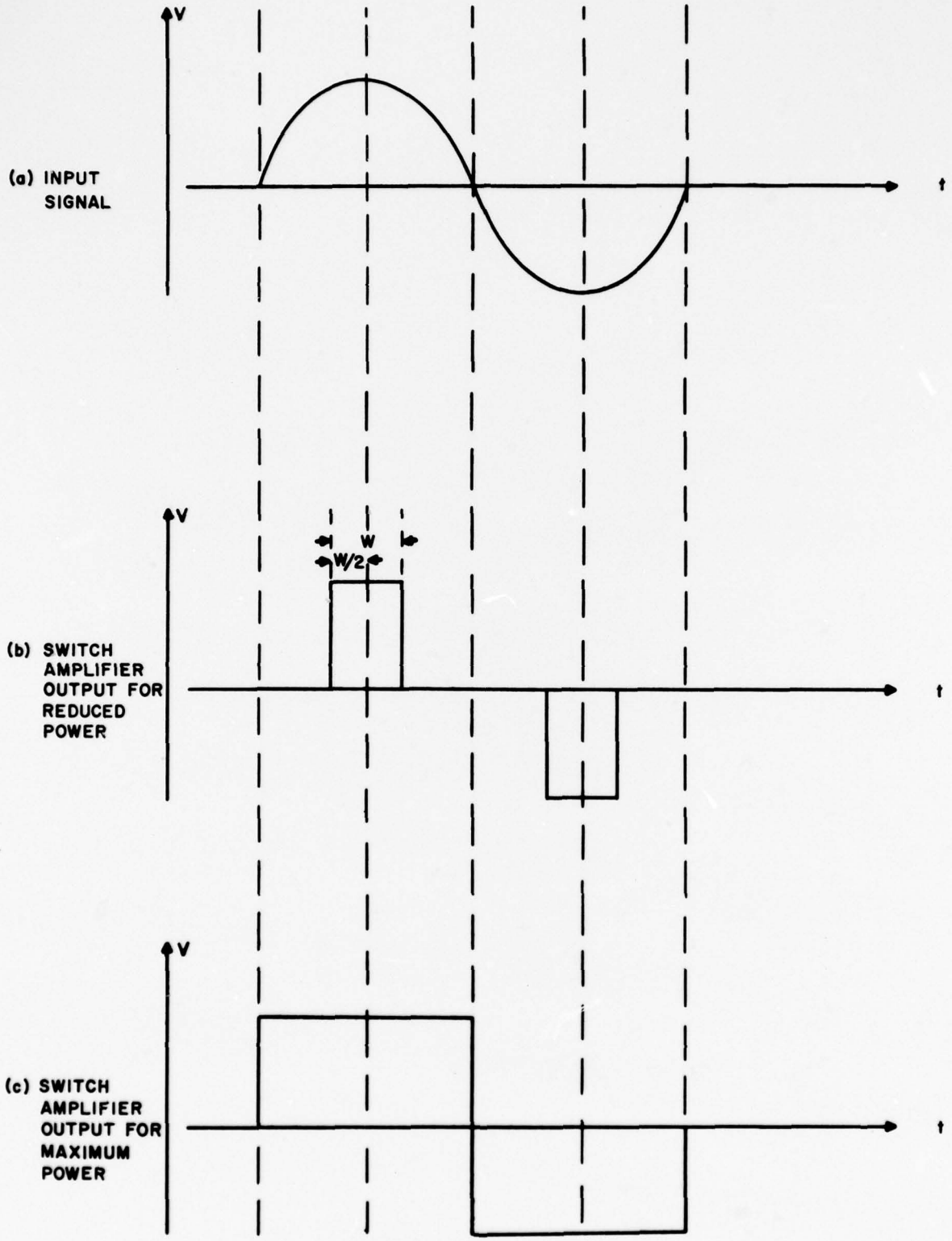


Figure 1. Switching Amplifier Waveforms

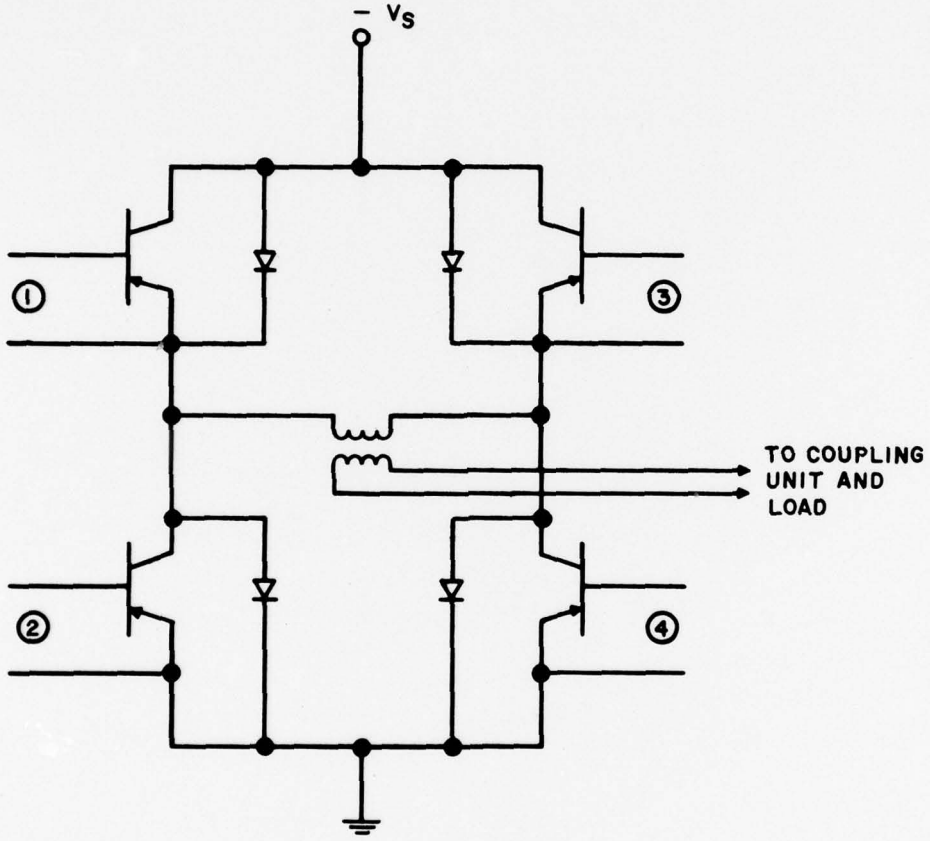


Figure 2. Basic Transistor Bridge Output Stage

Included in the output stage circuitry is a load coupling unit. A low pass or bandpass coupling unit is necessary when it is considered that the output voltage waveform of the bridge as shown in Figure 1 contains substantial harmonic content in addition to the desired signal fundamental frequency. The coupling unit is designed to present a high impedance to the amplifier at all frequencies except those in the fundamental frequency range, and hence, only fundamental current flows in the load despite the high harmonic content in the amplifier output voltage waveform. A series resonant LC network as shown in Figure 3 has a desirable impedance characteristic, the coupling circuit produces an overall acoustic output vs. frequency characteristic which is similar to a triple tuned filter network in the fundamental frequency range. For convenience, the coupling inductance was incorporated in the output transformer as secondary leakage inductance.

A portion of the system transmit-receive circuitry was included in the amplifier output stage. The TR circuitry is shown in Figure 4 and is composed of a diode D_1 and diode pair D_2, connected in the amplifier output transformer secondary. During the transmit phase of system operation diode pair D_2 is a low impedance and delivers the amplifier output power to the transducer load. Diode D_1 during this time is non-conducting. When the receiving function is desired diode D_1 is forward biased by the external TR control, and this shunts the output transformer secondary to the system common. The diode pair D_2 is non-conducting inasmuch as the received signal voltage is too small in magnitude to forward bias the diodes. Hence, the transducer received voltage appears at the receiver input terminals.

4. Power Control and Amplifier Input Circuitry

The amplifier input circuitry must provide suitable signals to drive the output bridge switching transistors in accordance with the waveforms of Figure 1 and in response to externally derived input signals which determine the frequency and amplitude of the desired amplifier output. Since the amplifier was required to produce a fixed output power for a given input signal condition over a range of load impedance variations, it was necessary to incorporate an automatic power level control function in the input circuitry. System considerations indicated that separate amplifier signal frequency and power level control input channels would

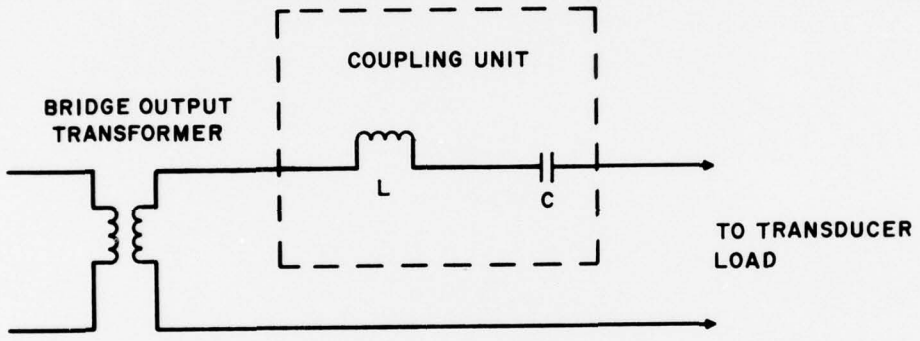


Figure 3. Amplifier Output Coupling Unit

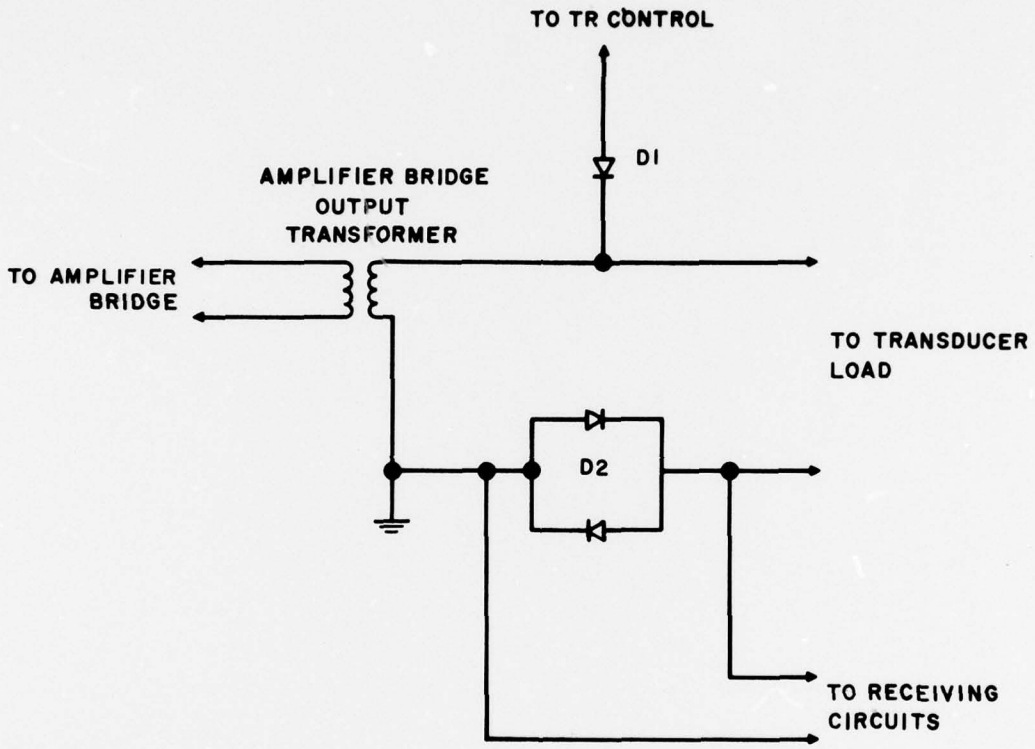


Figure 4. Amplifier Transmit - Receive Circuitry

permit substantial simplifications in the transmitter preamplifier and control sections. Accordingly, one of the amplifier inputs accepts a fixed amplitude square wave of voltage at the desired frequency, and the second input accepts a DC voltage level which is related to the amplifier output power level. The operation of frequency and power level channels is best described with the aid of Figures 5 and 6.

Figure 5 shows the circuitry associated with the signal frequency channel. A fixed amplitude square wave at the desired signal frequency is applied at the primary of the input transformer. Four windings are provided to drive the base-emitter electrodes of the bridge switching transistors. The winding polarities are arranged to provide paired operation of the transistors in the manner described previously, namely, transistor pair 1 and 4 operating in phase with each other and out of phase with the opposing transistor pair 2 and 3. It should be noted that the midpoint connection of windings W_2 and W_4 which control the associated transistors 2 and 4 may be connected to ground, and a square wave will be produced at the amplifier output transformer. On the other hand, if the midpoint connection is returned to a positive voltage whose magnitude is in excess of the square wave amplitude of W_2 and W_4, then the base electrodes of transistors 2 and 4 will be reverse biased and zero output power will be produced by the amplifier. It is, therefore, possible to control the switching function of transistors 2 and 4 by means of the midpoint connection of W_2 and W_4 and consequently, control the output power of the amplifier. In order to produce the output waveform of Figure 1, it is necessary to apply a positive voltage at the W_2-W_4 midpoint connection during the "off" interval of each half cycle as indicated in Figure 1, and to ground the midpoint connection during the remaining intervals.

Figure 6 shows the circuitry which connects the W_2 - W_4 midpoint terminal either to a positive voltage or to ground in accordance with the requirements set forth above. A positive voltage is applied at the W_2 - W_4 terminal when transistor Q_1 conducts, and the terminal is connected to ground when Q_2 conducts. The connections are arranged so that when Q_1 conducts, Q_2 is reverse biased into non- conduction by the diode D potential, produced by the current flow from transistor Q_1 through diode D. Transistor Q_1 is switched "on" and "off" by the signal from amplifier stages Q_3 and Q_4. Proper timing of the switching action is achieved by the

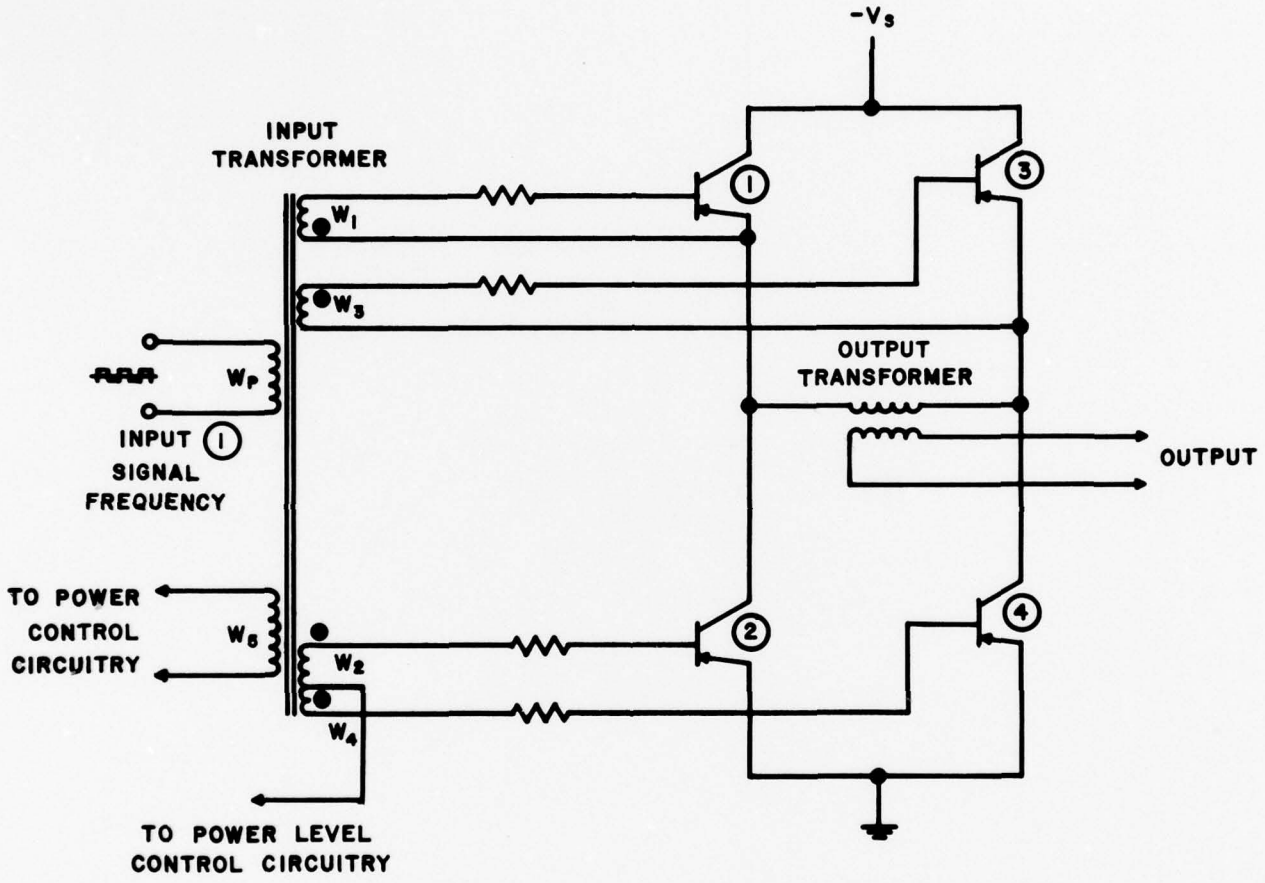


Figure 5. Amplifier Signal Input Circuitry

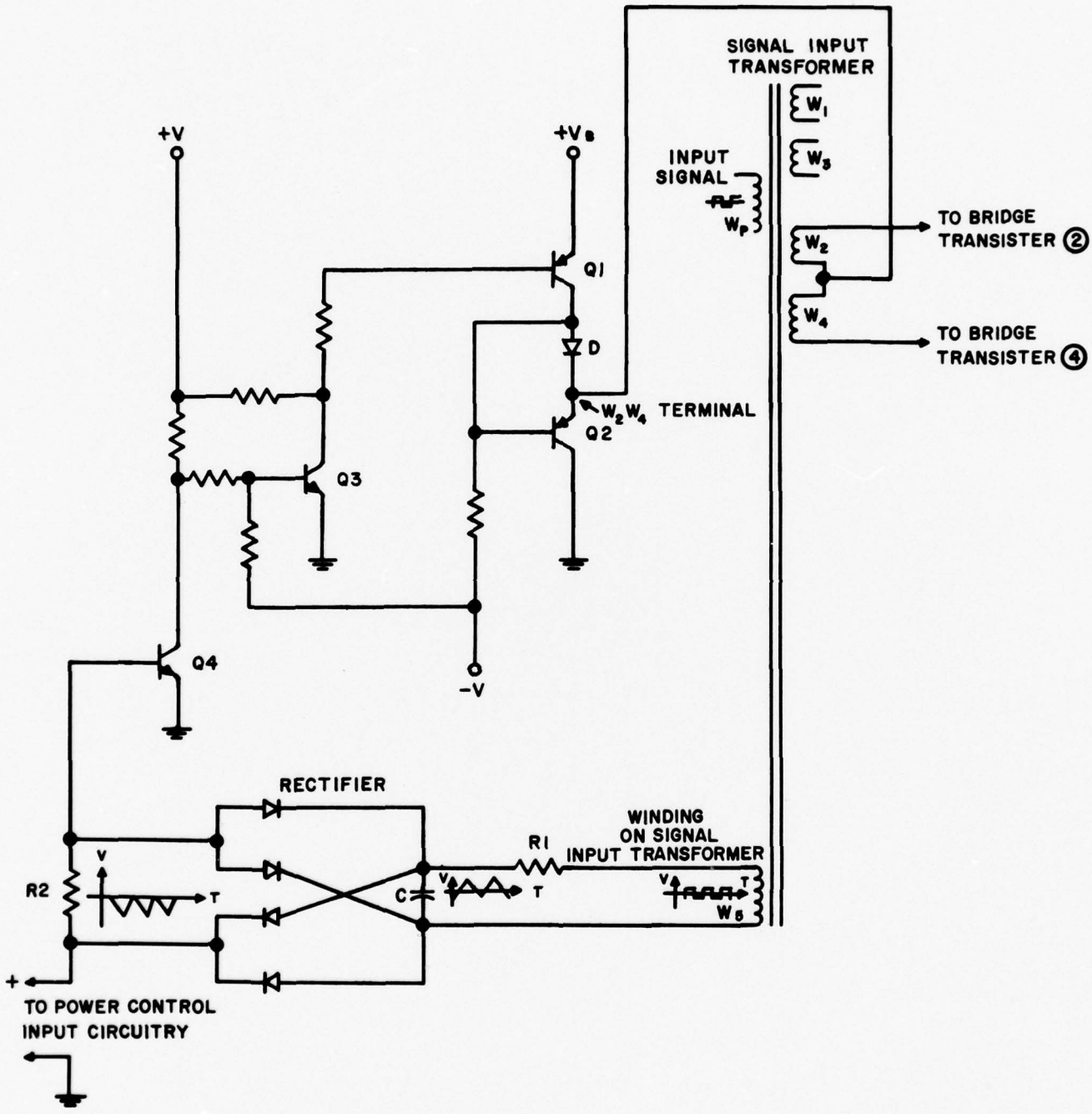


Figure 6. Amplifier Power Control Circuitry

circuitry composed of R_2, a full wave rectifier, capacitor C, resistor R_1, and a timing winding W_5 located on the amplifier signal input transformer. The action of the timing circuitry may be described with the aid of the waveforms illustrated in Figure 7. The input square wave (7a) is applied across the integrating network composed of R_1 and C. Waveform (7b) appears across C and has the time or phase relationship as shown. The capacitor voltage is rectified by the full wave rectifier and applied across resistor R_2. Waveform (7c) appears at R_2. If the positive terminal of R_2 were returned to ground, the base of NPN transistor Q_4 would always be negative in accordance with waveform (7c), and no current would flow in the Q_4 collector circuit. Consequently, Q_3 would conduct and Q_1 would return this W_2-W_4 terminal to the positive potential V_B. Therefore, no output would appear at the amplifier bridge output terminals. If rather than grounding R_2, a positive voltage is applied to R_2, then the base line of the waveform (7c) diagram is shifted as indicated, and Q_4 conducts for an interval of time during each signal half cycle for a period determined by the relative magnitudes of the applied positive R_2 voltage and the triangular wave. The timing of the conduction periods with respect to the input wave is as shown in Figure 7. Conduction of transistor Q_4 results in non-conduction of Q_3, and this by virtue of the Q_1 Q_2 action grounds the W_2 - W_4 terminal. A partial square wave is, therefore, produced by the amplifier bridge output stage. Figure 7d shows the W_2 - W_4 terminal voltage waveform under this condition, and Figure 7e shows the resulting amplifier output waveform. It should be noted that the time duration of the output half cycle pulses may be varied from zero to a full half cycle period, by simply changing the positive potential at R_2 from zero to a value larger than the peak value of waveform 7c. Inasmuch as the duration of the output pulses determines the amplifier output power it is seen that the potential at R_2 controls the power level of the amplifier.

Among the functions that must be performed by the amplifier was the requirement that nearly constant output power should be delivered even though comparatively large load impedance variations occur during operation. The power control input circuit of Figure 8 performs the constant power level function. It adjusts the positive potential, of R_2 Figure 6 in response to a DC power level control signal at the input of the amplifier and a feedback voltage derived from the amplifier output. The action of the circuit may be described by considering various input signal

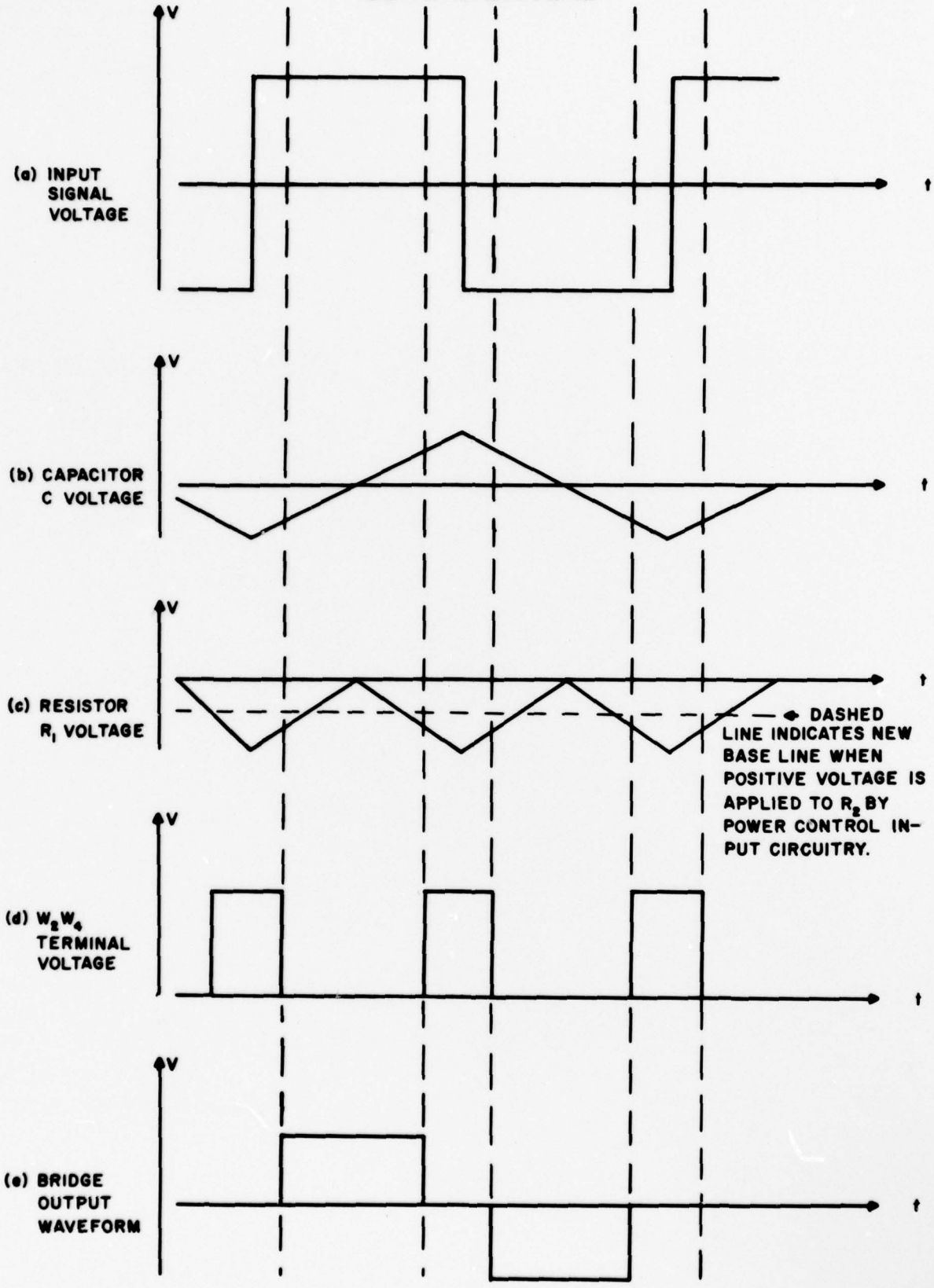


Figure 7. Amplifier Power Control Waveforms

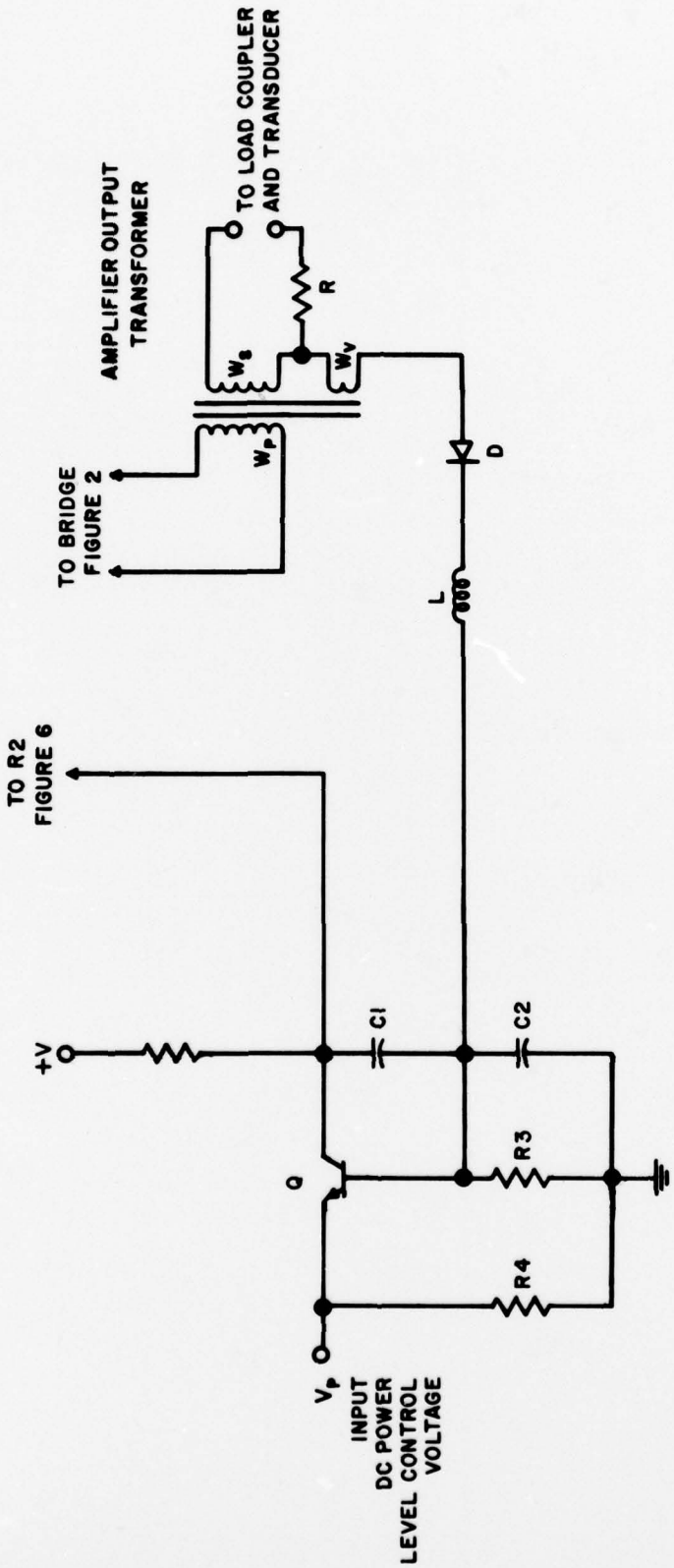


Figure 8. Power Control Input Circuit

conditions. When the DC input control signal is negative the transistor Q conducts, and this reduces the collector potential to zero or a negative value assuming a sufficiently negative value of input. From previous discussion, a zero DC potential at R_2 results in zero output at the amplifier output terminals. If the potential at the DC control input is changed to a positive value, the collector current flow of transistor Q is reduced. This allows the voltage at R_2 to increase to a more positive value, and the amplifier output power increases correspondingly. The amplifier output would increase to maximum output were it not for the feedback voltage developed across R_3. It opposes the original input DC control voltage, and eventually a balance condition results whereby the amplifier output power attains a value sufficient to develop a feedback voltage which is approximately equal to the DC control voltage.

Nearly constant output power is maintained for a fixed DC control voltage despite substantial load impedance changes through the action of the feedback loop circuitry composed of load current sensing resistor R, winding W_v, diode D, and low pass filter LC_2. As amplifier load current develops, voltage builds up across the current sensing resistor R. This voltage is added to a fraction of the load voltage appearing across winding W_v. The combined voltage is rectified by diode D, filtered by the low pass filter LC_2, and applied to base resistor R_3. A simple computation shows that a nearly constant power condition is achieved with the Figure 8 circuitry. If V_o is the output voltage and I_o is the output current, then $R_L = V_o/I_o$, and the amplifier output power if $P_o = V_o I_o$. From the amplifier equilibrium condition

$$kV_o + RI_o = V_p \tag{1}$$

where k is the fraction of output voltage appearing at winding W_v and V_p is the input DC power control voltage. These relations may be combined to give the amplifier power,

$$P_o = \frac{V_p}{R_L} \frac{1}{(k + \frac{R}{R_L})^2} \tag{2}$$

If k is arranged to be equal to R/R_{LN} where R_{LN} is the nominal value of load resistance, then (2) becomes

$$P_o = \frac{V_p^2}{R_L R^2} \quad \frac{1}{\left(\frac{1}{R_{LN}} + \frac{1}{R_L}\right)^2} \tag{3}$$

It may be noted that the amplifier output power is proportional to the square of the input DC power control voltage V_p. An indication of the insensitivity of power output with respect to load changes may be seen by considering the power output when the load R_L varies from $R_{LN}/2$ to $2R_{LN}$. From (3) the output power P_o for a load of $R_{LN/2}$ is

$$P_o^1 = 2\, V_P{}^2 R_{LN}/9R^2 \tag{4}$$

when $R_L = R_{LN}$

$$P_o^{11} = V_P{}^2\, R_{LN}/4R^2 \tag{5}$$

and when $R_L = 2R_{LN}$

$$P_o^{111} = 2V_P{}^2 R_{LN}/9R_2 \tag{6}$$

Hence, the variation from the power for a nominal load value may be expressed by

$$P_o^1 \,/\, P_o^{11} = 8/9 \approx 88\% \tag{7}$$

Thus, the output power of the amplifier should not vary more than 12 percent from the power delivered to a nominal load over a 4 to 1 load variation. The load which will be connected to this amplifier is not expected to exceed a 3 to 1 variation in impedance, and hence, the deviation from nominal output power should be less than that given by equation (7).

5. Overload Protection Circuit

An instantaneous overload protection circuit was deemed necessary to prevent failures due to momentary excessive bridge currents which might result from transient load conditions. The circuit of Figure 9 was incorporated to turn "off" the number

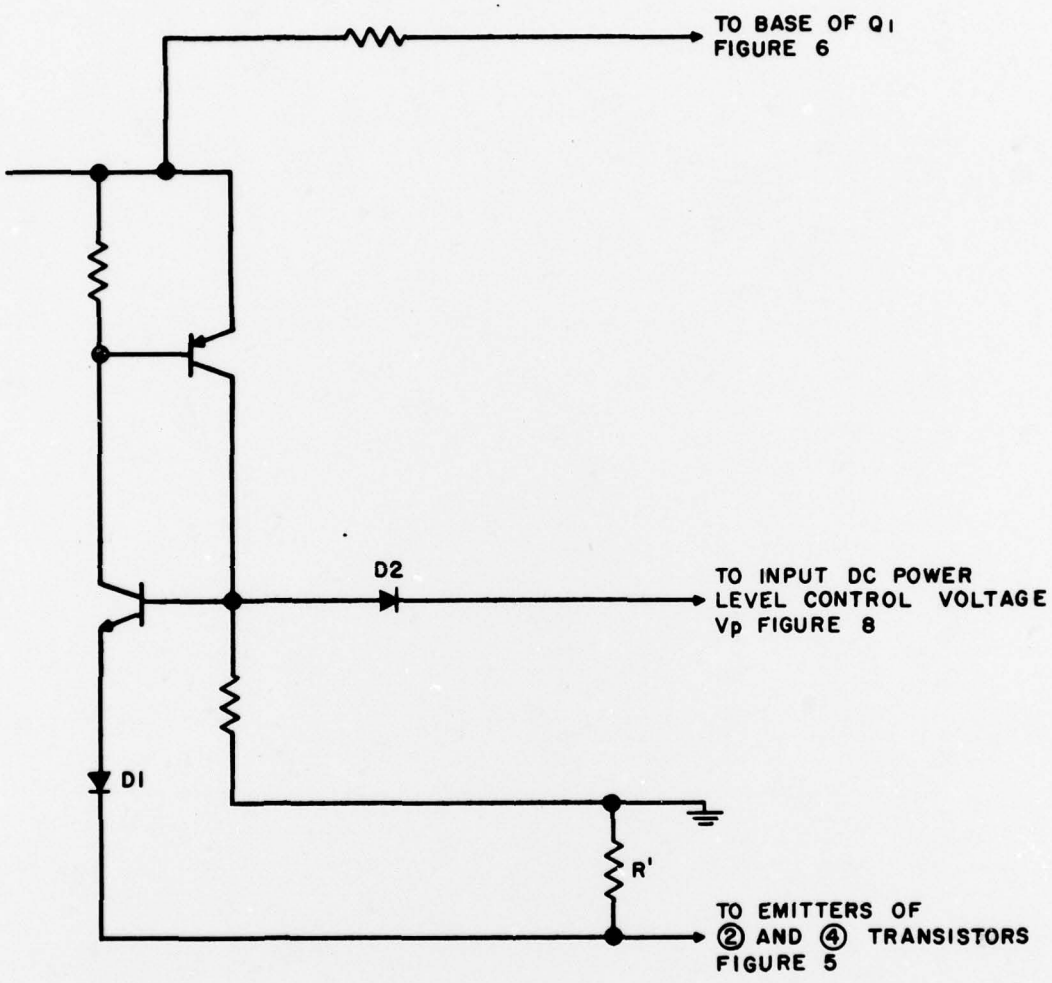


Figure 9. Overload Protection Circuit

2 and 4 bridge transistors of Figure 5 when excessive current exists in the bridge. A current monitoring resistor R^1 is incorporated in the bridge ground return lead to develop a voltage proportional to the total bridge current. This voltage is applied to a switching circuit composed of an NPN and PNP transistor pair. When the voltage developed across the current sensing resistor R^1 exceeds the combined voltage drops of diode D_1 and the emitter-base diode of the NPN transistor, the NPN transistor and its PNP mate conduct. Since the output of each transistor feeds the input of the other transistor of the pair, it is seen that conduction will continue in both transistors even if the original input voltage from R^1 is removed. The switching action is very rapid and may be initiated with a very short duration input voltage pulse from R^1. Once the transistor pair is switched into the conducting condition current flows to the base of transistor Q_1 of Figure 6, and this results in the application of a positive bias voltage V_B to terminal W_2 - W_4. The bridge transistors number 2 and 4 are thereby turned "off", and the bridge current returns to zero. It will remain zero as long as the protection circuit is conducting. In order to reset the overload circuit, it is necessary to apply a negative voltage to the base of the NPN transistor. This voltage is available at the input DC power level control terminal during the non-operating period of the power amplifier. A diode D_2 couples this negative reset voltage to the overload circuit and prevents the normal positive DC control voltage from actuating the overload function.

6. Experimental Results

Figure 10 shows the circuit of the complete amplifier. Breadboard tests of the amplifier were conducted to evaluate the performance with actual transducer loads and with electrical loads which simulate a transducer load. The simulated transducer load circuit is shown in Figure 11. It was driven to power levels of 900 watts. Figure 12 shows current and voltage waveforms at pertinent points in the amplifier and load circuits. The tests were repeated with an actual transducer load, and a power level of 750 watts was achieved. A series of tests was initiated at the end of the reporting period to evaluate the constant load power function, the overload protection circuit, and the performance with respect to signal frequency and temperature. This work is continuing and will be reported at the end of the next reporting period.

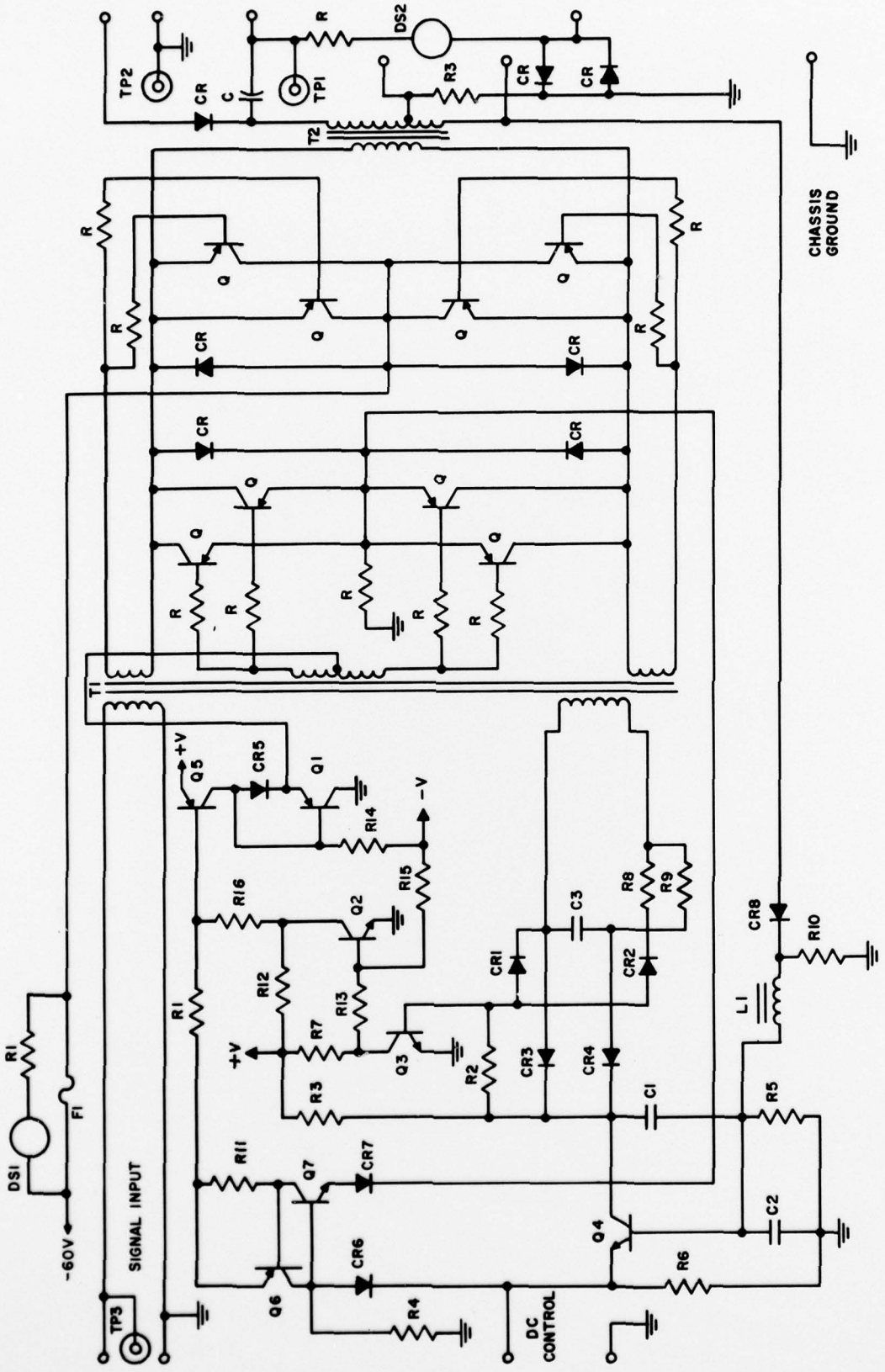


Figure 10. Power Amplifier Module Schematic

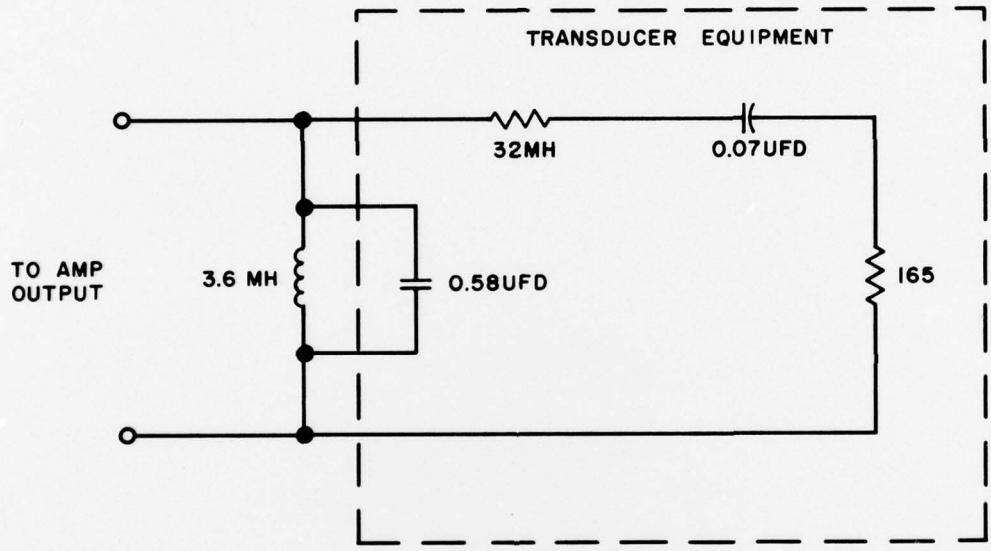
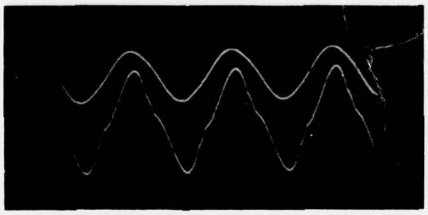


Figure 11. Simulated Transducer Load Circuit

TOP- BRIDGE VOLTAGE-50 V/CM
BOTTOM-BRIDGE CURRENT-20 A/CM

A. BRIDGE VOLTAGE (1 SIDE)-BRIDGE CURRENT



TOP-LOAD VOLTAGE-500 V/CM
BOTTOM-LOAD CURRENT-2 A/CM

B. LOAD VOLTAGE-LOAD CURRENT WAVEFORMS

Figure 12. Amplifier Current and Voltage Waveforms with Simulated Transducer

7. Input and System Control

To obtain increased reliability and circuit simplification it was decided to develop the square wave for driving the power amplifier bridge, in modules capable of driving several bridges rather than duplicating the circuitry for each power amplifier.

To this end a driving amplifier capable of providing the signal to either two or six power amplifiers (for directional or omnidirectional modes respectively) was designed. (Figure 13 shows the circuit tested.) The power level of the drive signal for the input of each power amplifier was set at approximately 35 watts for each bridge module in directional transmission and about 25 watts per module for the omnidirectional mode. To provide reliable operation an amplifier capable of providing up to 240 watts was designed and tested.

The input signals for the driver amplifier are provided by a 2 phase to 12 phase transformer. This transformer is wound in such a fashion that the correct phase for beam formation is fed to each of the driver amplifiers. The driver amplifier converts the sinusoidal output of the transformer to a square wave which is amplified to the level required by the power amplifier.

The transformers are driven by low power, Class A amplifiers, Figure 14, which raise the level of the input signal to the transmitting system to a level sufficient to drive the 2 phase to 12 phase transformers.

The output signal power level is determined by the amplitude of the sinusoidal signal applied to the Class A amplifiers. As described previously, the power amplifier module requires that the power level control be a DC voltage. Consequently a level detector has been incorporated in the system to set the power level of the output signal and simultaneously provide the required output signal level shading as required for proper beam formation. The circuit for providing this function is described in Figure 15.

Application of the drive and power level control to the appropriate power amplifiers, and thus to the appropriate transducer elements for the purpose of directional transmission is to be accomplished by means of a step switch in a manner previously described in the Second Interim Report (Figure 3).

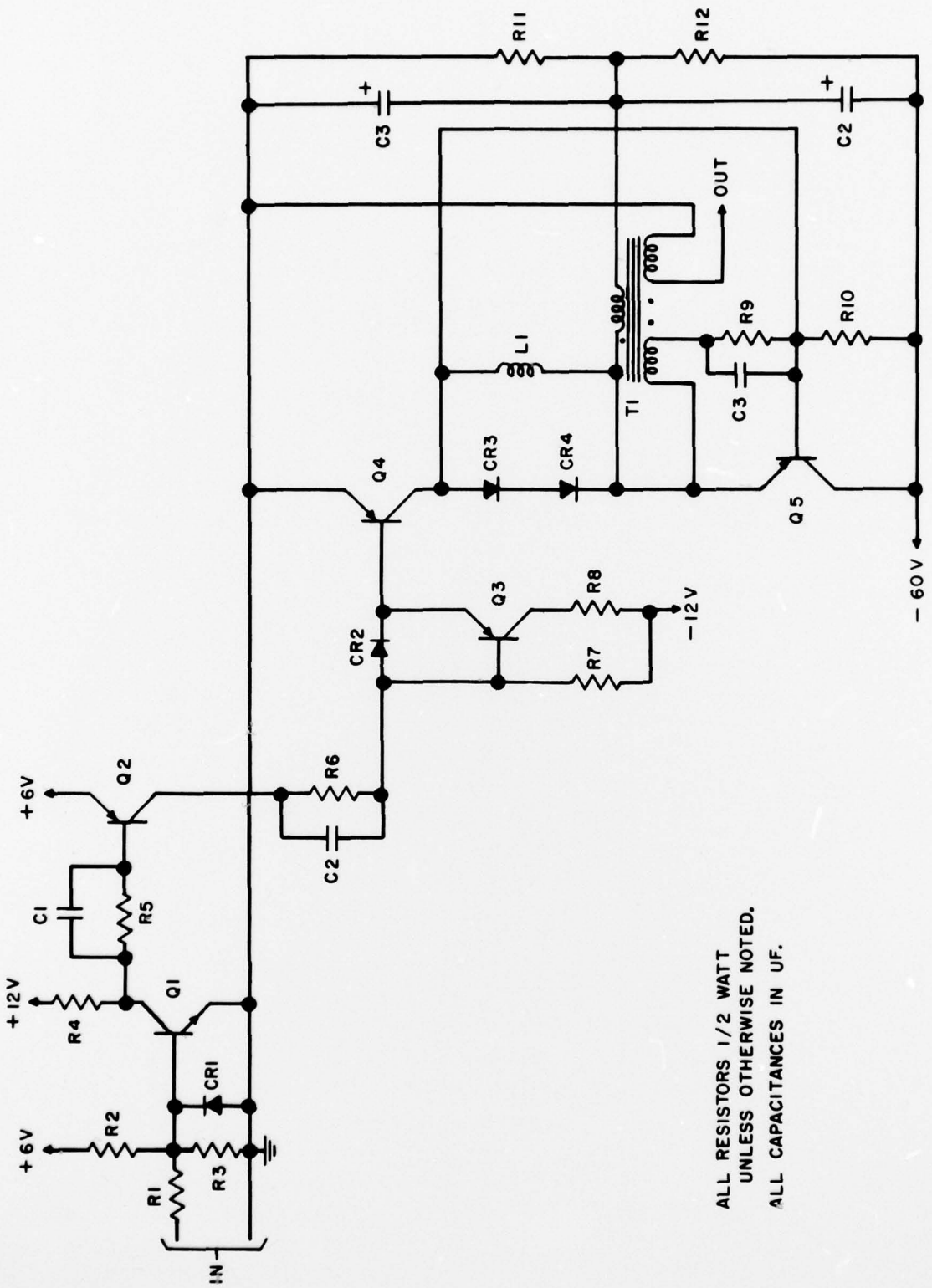


Figure 13. AN/SQS-26 ( ) Driver Amplifier

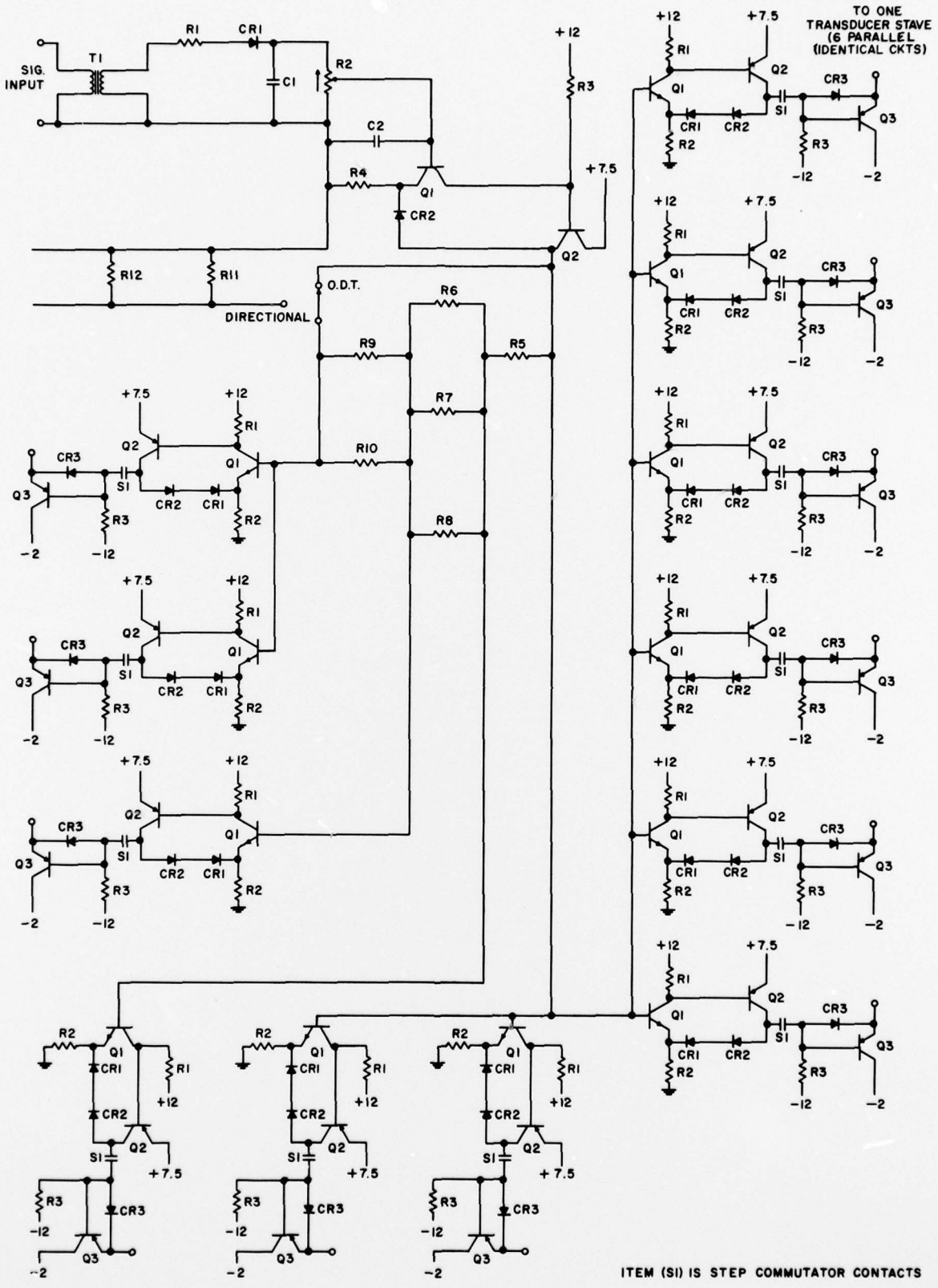


Figure 14. AN/SQS-26 ( ) DC Control Driver

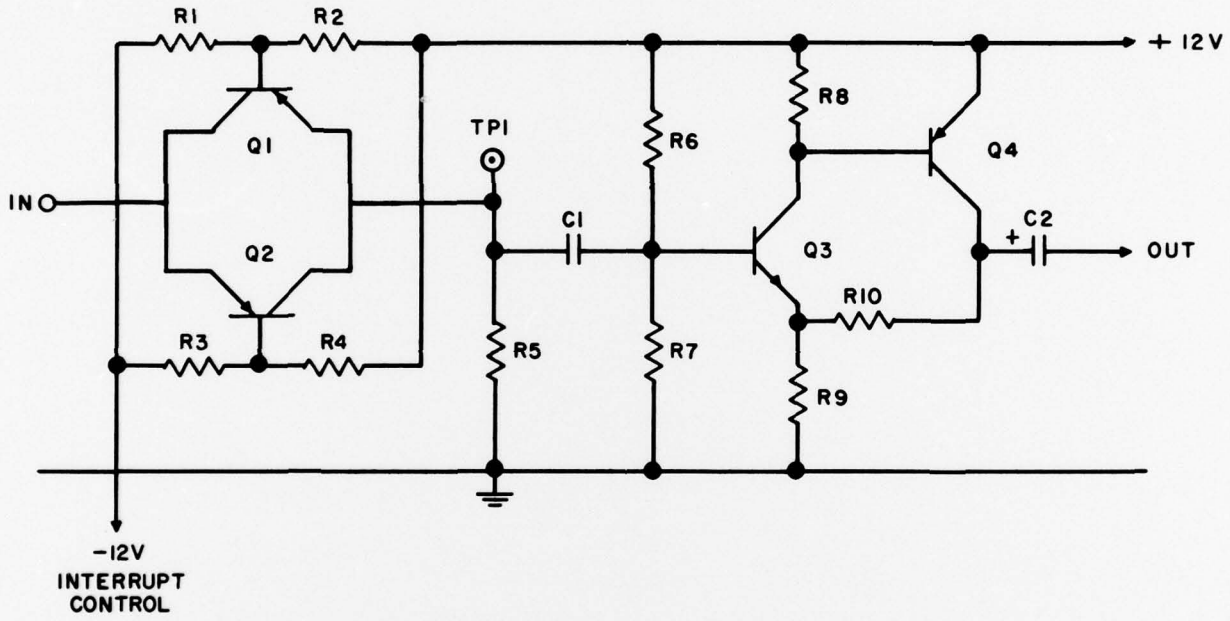


Figure 15. AN/SQS-26 ( ) Linear Amplifier

Although the step switch appears to be the simplest and most reliable means of accomplishing the control of the direction of transmission, the availability of such a device to meet operational requirements is not known. Therefore, a parallel approach to obtain the same results was undertaken. The method of providing the signals to the appropriate power amplifiers would be by means of semiconductors or relays which are driven by logic and computer circuitry.

An investigation of the relative merits of the several possible methods of obtaining the desired results and an evaluation of the components, resulted in the selection of a relay to perform the switching function.

Relays were chosen over transistors because one multipole relay can switch all 8 decks together, whereas 8 transistors would be required. To perform the same commutation with transistors would require about 1400 transistors. Furthermore, considerably greater driving power would be needed to operate transistors. Each 12-pole relay requires approximately 50 ma at 28V to operate, independent of the current the contacts must carry. Assuming each of the contacts had to carry 2.5 amperes; 8 decks would handle 20 amperes, with an effective current gain of 20A/50 ma = 400. Transistors could be assumed to have a current gain no greater than 20 or 30 so approximately 10 times as much driving current would be required. In addition, the current carried by the relay contacts can be increased up to their rated limit (which is considerably higher than most transistors) without increasing the drive; with transistors, either more drive or higher gain would be necessary. The present number of components (168 12-pole and 72 single-pole relays, and approximately 400 diodes in the driving logic) is not guaranteed to be the minimum possible number; however, considerable study of the problem has not indicated a simpler approach.

PART II

PROGRAM FOR NEXT INTERVAL

Breadboard evaluation of the drive and control circuits individually and as a unit will be completed and a nine module test array will be constructed. Tests will be initiated to evaluate the modules when operated into transducers with various phase angles applied to each module.